1. A semiconductor device electrostatic discharge protection structure on a substrate comprising:

a first doped region of opposite dopent than said substrate extending down from the surface of said substrate;

a heavily doped second region with associated electrical contact area within said first doped region of similar dopent to said first doped region;

a heavily doped third region with associated electrical contact area within said first doped region of opposite doping than said first doped region;

a first isolation element at the surface region lateral boundaries between said first doped region and said substrate adjacent to said heavily doped second region;

a heavily doped fourth region with associated electrical contact area within said substrate of opposite doping than said substrate;

a heavily doped fifth region with associated electrical contact area within said substrate of similar dopent to said substrate;

a second isolation element adjacent to said fifth doped region and on opposite side from said fourth doped region;

a first insulation element layer on said substrate surface except on said electrical contact areas;

a first electrical conduction element connecting said second and third doped regions and to a first voltage source;

a second electrical conduction element connecting said fourth and fifth doped regions and to a second voltage source;

a top passivation layer overlaying said device surface.

2. The protection structure of claim 1 wherein said substrate consists of P doped semiconductor

material.

3. The protection structure of claim 1 wherein said first doped region is N doped with a concentration between 1E16 and 1E18 a/cm^3, and forms a N-well within said substrate.

4. The protection structure of claim 1 wherein said second and said fourth heavily doped regions are N doped to a concentration between 1E19 and 1E21 a/cm^3..

5. The protection structure of claim 1 wherein said third and said fifth heavily doped regions are P doped to a concentration between 1E19 and 1E21 a/cm^3.

6. The protection structure of claim 1 wherein said electrical contact areas of said second, third, fourth and fifth heavily doped regions contain a refractory metal salicide.

7. The protection structure of claim 1 wherein said first insulation element layer consists of thermally deposited silicon dioxide to a thickness of between 1000 and 3000 Å to block the formation of said salicide in unwanted areas.

8. A semiconductor device electrostatic discharge protection structure on a substrate comprising:

a first doped region of opposite dopent than said substrate extending down from the surface of said substrate;

a first isolation element at the surface region first lateral boundary between said first doped region and said substrate;

a heavily doped second region with associated electrical contact area within said first doped region of similar dopent to said first doped region;

a heavily doped third region with associated electrical contact area within said first doped region of opposite dopent to said first doped region;

a heavily doped fourth region with associated electrical contact area within said substrate of opposite doping than said substrate;

a heavily doped fifth region with associated electrical contact area within said substrate of similar dopent to said substrate;

a heavily doped sixth region of same dopent as said doped second region located at the surface region second lateral boundary of said first doped region and said substrate;

a second isolation element adjacent to said fifth doped region and on opposite side from said fourth doped region;

a first gate element overlying said surface region between said fourth doped region and said sixth doped region;

a first insulation element layer on said substrate surface except on electrical contact areas;

a first electrical conduction element connecting said second and third doped regions to a first voltage source;

a second electrical conduction element connecting said fourth and fifth doped regions and said first gate element and to a second voltage source;

a top passivation layer overlaying said device surface.

9. The protection structure of claim 8 wherein said substrate consists of P doped semiconductor material.

10. The protection structure of claim 8 wherein said first doped region is N doped with a concentration between 1E16 and 1E18 a/cm^3, and forms a N-well within said substrate.

11. The protection structure of claim 8 wherein said second, said fourth and said sixth heavily doped regions are N doped to a concentration between 1E19 and 1E21 a/cm^3.

12. The protection structure of claim 8 wherein said third and said fifth heavily doped region are P doped to a concentration between E19 and E21 a/cm^3.

13. The protection structure of claim 8 wherein said sixth heavily doped region forms an FET

with said heavily doped fourth region and said first gate element.

14. The protection structure of claim 8 wherein said first insulation element layer consists of thermally deposited silicon dioxide to a thickness of between 1000and 3000 Å to block the formation of said salicide in unwanted non-contact areas.

15. A semiconductor device electrostatic discharge protection structure on a substrate comprising:

an insulating layer element under the surface of said substrate;

a single crystal active device region between said insulating layer and said substrate surface;

a first doped region with associated electrical contact area within said active device area extending down from the surface of said substrate to said insulating layer;

a first isolation element at the surface region first lateral boundary between said first doped region and said active device region extending down to said insulating layer;

a heavily doped second region with associated electrical contact area within said first doped region of similar dopent to said first doped region;

a heavily doped third region with associated electrical contact area within said first doped region of opposite doping than said first doped region;

a doped fourth region adjacent to said first doped region extending from said substrate surface down to said insulating layer and of opposite dopant than said first doped region;

a heavily doped fifth region with associated electrical contact area within said fourth doped region of opposite dopant than said fourth doped region;

a heavily doped sixth region with associated electrical contact area within said fourth doped region of similar dopant than said fourth doped region;

a second isolation element adjacent to said sixth doped region and on opposite side from said fifth doped region between said fourth doped region lateral boundary and said active device area;

a first insulation element layer on said substrate surface except on said electrical contact areas;

a first electrical conduction element connecting said second and third doped regions and to a first voltage source;

a second electrical conduction element connecting said fifth and sixth doped regions and to a second voltage source;

a top passivation layer overlaying said device surface.

16. The protection structure of claim 15 wherein said first doped region is N doped with a concentration between E16 and E18 a/cm^3, and forms a N-well within said active device region.

17. The protection structure of claim 15 wherein said second and said fifth heavily doped regions are N doped to a concentration between E19 and E21 a/cm^3.

18. The protection structure of claim 15 wherein said third and said sixth heavily doped regions are P doped to a concentration between E19 and E21 a/cm^3.

19. The protection structure of claim 15 wherein said first insulation element surface layer consists of thermally deposited silicon dioxide to a thickness of between 1000 and 3000 Å to block the formation of said salicide in unwanted areas.

20. A method of fabricating a silicon controlled rectifier electrostatic discharge protection device on a semiconductor substrate comprising:

forming a first doped region of opposite dopant than said substrate extending down from the surface of said substrate;

creating multiple isolation elements within said semiconductor substrate on either side of said silicon controlled rectifier device active area;

forming a heavily doped second region with associated electrical contact area within said first doped region of similar dopant to said first doped region and forming a similar doped fourth region within the substrate area;

forming a heavily doped third region with associated electrical contact area within said first doped region of opposite doping than said first doped region, and forming a similar doped fifth region in the substrate area;

forming a first insulation layer on the surface of said silicon controlled rectifier device everywhere except for said electrical contact areas;

Evaporating and annealing a refractory metal blanket over said silicon controlled rectifier device surface including on top of said first insulation surface layer;

Removing unwanted said refractory metal from said silicon controlled rectifier device surface non-electrical contact areas and performing a stabilization anneal;

continuing said silicon controlled rectifier device processing to completion including creating first and second conductor elements and a passivation layer.

21. The method according to claim 20 whereby said first doped region is donor doped with phosphorous with a dosage between E15 and E17 a/cm^2 with an energy between 30 and 80 KeV to produce a N-well.

22. The method according to claim 20 whereby said second and fourth heavily doped regions with associated contact areas are doped with a donor dopant such as arsenic with a dosage between 1E13 and 1E15 a/cm^2 and an energy level between 20 and 40 KeV.

23. The method according to claim 20 whereby said third and sixth heavily doped regions are

doped with an acceptor dopant such as boron with a concentration of between 1E12 and 1E13 a/cm^2 and with an energy level between 40 and 80 KeV.

24. The method according to claim 20 whereby said first insulating layer is thermally grown SiO_2 at a temperature between 700 and 1100 °C to a thickness between 1000 and 3000 Å.

25. The method according to claim 20 whereby said refractory metal blanket consists of titanium or tungsten or tantalum or molybdenum

26. The method according to claim 20 whereby said conducting elements are comprised of aluminum or similar metallurgical material.